Electronic systems are becoming increasingly portable and getting miniaturised as a result of advanced integrated circuits, miniaturized power sources and high density I/Os. The flip side to scaling is that it creates ICs that are more susceptible to transient voltages due to thinner oxides and smaller metallization traces. The ideal method of transient voltage suppression is to clamp the transient voltage with a transient voltage suppressor (TVS). TransZorb and Multilayer Varistors (MLVs) are an ideal choice of TVS’s since they clamp voltage in their ON state diverting the surge away from the sensitive electronics, and act as an EMI filter in their off state. This paper will concentrate on characterizing the ESD performance, both clamping and filtering effects provided by these devices.

1.0 Introduction

Normal day-to-day activities can cause people to build up static electricity, called triboelectric charging, which might later be transferred to objects like electronic devices and circuits. The transfer of electrical charge from object at higher electrical potential to an object at lower electrical potential is referred to as electrostatic discharge, resulting ESD transient pulse. If the ESD pulse finds its way into the electronic devices, the circuitry inside can be physically damaged. ESD can lower product reliability. To help reduce losses due to ESD, chip manufacturers incorporate TVS structures into their integrated circuitry.

The next level problem occurs when the electronic product transfers from the manufacturing environment to final use. The level of ESD the end user can generate and introduce to the electronic device is much more severe than the level found in the controlled manufacturing environment. Consequently, the focus of ESD protection has shifted from chip hardening to system hardening. The protection options available to the designer include isolation circuits, filtering circuits, and suppression components, such as multilayer varistors, silicon diodes, and the newly introduced polymer-based suppressors.

Suppression components protect the circuit by clamping the ESD voltage to a level that the circuit can survive. Connected in parallel with the signal lines, the suppressors clamp the ESD voltage and shunt the majority of the ESD current away from the signal line to the appropriate reference, generally chassis ground.

2.0 Protection Circuit Design Considerations

Electronic design trend is toward higher data throughput and faster signal speeds. This adds to the complexity of protection circuit design. Basically, ESD protection falls into two categories: protection during manufacturing, and protection in the "real-world" environment.

On-chip protection circuit design aspects can be broadly classified in to two categories, viz. to increase chip yields in IC manufacturing and board assembly environments, by following the standard available models such as Charged Device Model (CDM), the Machine Model (MM), and the Human Body Model. But the severity of ESD in the "real-world" environment experienced by interface circuits is much higher compared to models used during manufacturing. The real world ESD transients are specified in the EN 61000-4-2 test methodology. It's important to remember that survival through the manufacturing process does not guarantee survival in the field. This demands for the incorporation of external ESD protection circuit designed to meet EN 61000-4-2 test methodology.
2.1 ESD Current Pulse of EN 61000-4-2 – Its Power Spectral Density

The current pulse of EN 61000-4-2 ESD contact discharge is specified in the time domain. The specified current pulse metrics are: first peak of ESD current pulse, (10%-90%) rise time and “tail currents” at 30ns and in 60ns. The key metric with respect to the frequency bandwidth is the rise time. The rise time of the ESD pulse is equal to 0.8ns. This ESD current pulse can be mathematically modelled by equation (1) given below [Reference 1]. Two components of the current can be distinguished in the ESD current pulse. The fast-varying component, represented by the first summand in equation (1) and the dashed red line in Figure 3, is due to arc discharge of a small capacitance between the metal tip held by a person approaching device and the device. The slow-varying component, represented by the second summand in equation (1) and the dotted blue line in Figure 1, results from discharge of a larger body capacitance of a person.

\[
i(t) = \frac{I_1}{k_1} \left( \frac{t}{\tau_1} \right)^n e^{-\frac{t}{\tau_3}} + \frac{I_2}{k_2} \frac{t}{1 + \left( \frac{t}{\tau_1} \right)^n} e^{-\frac{t}{\tau_3}}
\]

Where

\[
k_1 = \exp \left[ -\frac{\tau_1}{\tau_2} \left( \frac{n \cdot \tau_2}{\tau_1} \right)^{1/n} \right], \quad k_2 = \exp \left[ -\frac{\tau_3}{\tau_4} \left( \frac{n \cdot \tau_4}{\tau_3} \right)^{1/n} \right]
\]

The values of the parameters are for + 4kV charge voltage of the ESD are given in the table.

<table>
<thead>
<tr>
<th>( l_1 ) [A]</th>
<th>( l_2 ) [A]</th>
<th>( \tau_1 ) [ns]</th>
<th>( \tau_2 ) [ns]</th>
<th>( \tau_3 ) [ns]</th>
<th>( \tau_4 ) [ns]</th>
<th>( n )</th>
</tr>
</thead>
<tbody>
<tr>
<td>16.6</td>
<td>9.3</td>
<td>1.1</td>
<td>2</td>
<td>12</td>
<td>37</td>
<td>1.8</td>
</tr>
</tbody>
</table>

The PSD is the most common tool used in statistical signal analysis for description in the frequency domain. The PSD is a real positive function and has clear interpretation: power of a signal per unit frequency. The power spectral density (PSD) of a signal is the squared magnitude of its Fourier transform. For a sampled signal \( x(n) \) it can be calculated as:

\[
P_{xx}(\omega) = \frac{1}{N} \left| \sum_{n=0}^{N-1} x(n) e^{-j\omega f_s n} \right|^2 = \frac{1}{N} |X(\omega)X^*(\omega)|
\]

Where \( X(\omega) \) is the N-point fast Fourier transform of \( x(n) \), \( X^*(\omega) \) is the complex conjugate of \( X(\omega) \) and \( f_s \) is the sampling frequency. The PSD of ESD Current pulse is shown in Figure 2.

Fig. 2 Frequency Spectrum (PSD) of ESD Current Pulse
2.2 Generation of ESD Current Pulse - Circuit Simulations

Dual RLC model consists of two RLC sections that leads to a very fast rise time (less than 1 ns) initial current spike is shown in Figure 3 is used to generate the ESD current pulse as specified in EN 61000-4-2 test methodology.

The current pulse for discharge voltage of 10 kV is shown in Figure 4. There is a fast initial pulse of amplitude 37 A followed by the main discharge pulse of amplitude equal to 24 A (peak) meeting the standard EN 61000-4-2 test pulse requirements. This generator model is used in TransZorb simulations.

![Fig. 3 Dual RLC model ESD Pulse Generator](image)

![Fig. 4 Dual RLC model - ESD Current Pulse](image)

2.3 Single stage protection using TransZorb

The performance of single stage protection circuit is studied with ESD event (discharge voltage of 20 kV) as input (see Fig. 5) transient. The output voltage is clamped to study state 12 V (steady state) after an initial transient of 220 V (see Fig. 6). The peak current through the TransZorb is around 65 A and the waveform shows a second peak of around 45 A. [Reference 2]

![Fig. 5 Simulation Circuit of Single stage protection for ESD using TransZorb](image)

![Fig. 6 Voltage across and Current through TransZorb](image)

From this, a 20 kV ESD event gives rise to large transient currents in the protection devices and hence may be considered to be more damaging. Hence, the performance of protection circuits should be evaluated using an ESD simulator that generates the current waveform specified in standard EN 61000-4-2.

2.4 Effects of Parasitic Elements

Designers need to understand not only the suppression characteristics of ESD protectors, but also their package characteristics. It is very critical and important to consider the filtering effect provided by parasitic elements, especially the capacitance of ESD suppression devices and stray characteristics of placement of protection circuit with respect to the device to be protected. Make sure the ESD suppressor is a good fit with the circuit parameters (data rates, leakage current, and so on).
The inherent package capacitance of a suppressor could be used to the circuit designer's advantage. Where a high degree of separation exists between the signal frequency and any unwanted frequencies, like EMI "noise" and ESD transients, device capacitance provides the additional benefit of filtering. Essentially acting like a low-pass filter, the suppressor provides clamping functions for transient suppression and can provide EMI filtering against unwanted, high-frequency signals that couple into the protected data line.

Hence, in low frequency circuits, the high-capacitance multilayer varistors and diodes are ideal for ESD protection. They have the additional benefit of filtering. This additional advantage, however, becomes a limitation when the signal speed is increased. Data rates used present interfacing hardware/protocols exceed 100 Mbits/s. At these speeds, the capacitance that helped to eliminate unwanted noise will also begin filtering the data signals themselves, resulting in distorted data waveforms that can render a system inoperable.

The distortion takes the form of rounded leading and trailing edges of high/low state transitions resulting in timing issues. The circuit expects "high" and "low" states to be stable at specific times. As the transition time between states increases, the circuit can be caught sensing an incomplete transition, and data errors can be introduced into the system. From a circuit-protection standpoint, the goal is to provide ESD protection to the circuit and to maintain the integrity of the data, not to interfere with circuit operation.

### 3.0 Practical Characterization of TransZorb

A typical TransZorb PCB used in spacecraft to protect interface lines entering into the spacecraft Faraday cage, i.e., between external hardware and internal housekeeping hardware, is shown in Fig. 7. This PCB is mounted with seven numbers of 1N6037A TransZorb. Test setups used are shown in figure 8 and 9.

#### 3.1 Response of TransZorb to Standard Signals at different frequencies

The response of typical TransZorb (1N6037) used in spacecraft projects is evaluated by feeding different standard test waveforms shown in Fig. 10 through Fig. 14. This test data reveals the clear degradation of signal integrity due to presence of ESD transient protection devices across the line. The signal integrity of the system can't be compromised. Therefore, the capacitance of an ESD suppressor must be considered before adding it to the circuit design across the data lines of very high speed systems.

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**Fig.7** TransZorb Card used for tests  
**Fig.8** Test setup for frequency response

**Fig.9** Test setup for ESD transient response  
**Fig.10** Response of TransZorb – 100kHz Sinusoidal I/P
3.2 Response of TransZorb to ESD Current Pulse

Response of TransZorb to the ESD pulse is shown in Figure 15 and 16. From this response it is evident that input ESD transient is attenuated by filtering effect due to parasitic elements, dominantly by capacitance of TransZorb, not just by clamping alone.

Fig. 15 ESD pulse measured at Load of 300 Ohms paralleled with scope input impedance (1MΩ) without Tranzorb.

Fig. 16 ESD pulse measured at Load of 300 Ohms paralleled with scope input impedance (1MΩ) with Tranzorb. Measured Voltages are
4.0 Optimal placement of ESD suppressor

Optimal placement of ESD suppressors begins at the location of ESD penetration into the system. This strategy reduces the ESD voltage and current initially experienced by the circuit and attenuates the ESD pulse that propagates past the ESD suppressor. Design as much practical space as possible between the ESD suppressor and the protected chip.

By just following above recommendation, i.e., placing an ESD suppressor too far away from the circuit to be protected, can reduce its effectiveness. The parasitic inductance of interfacing harness length together with board trace inductance can cause an additional amount of voltage, or "overshoot," on the chip. To avoid this, the second level TVS device with lower ratings can be placed as close to the protected line as possible.

The bottom line is that selecting an ESD "solution" is no longer as simple as choosing a suppressor that's rated for the operating voltage of the circuit. An effective solution now takes into account the layout of the circuit board, as well as the non-suppression electrical characteristics of the ESD suppression devices.

5.0 Conclusion

Design considerations of ESD protection circuit discussed. Importance of EN6100-4-2 defined current pulse is brought out. Transient Voltage Suppressor is to be chosen to withstand the current pulse metrics defined in EN6100-4-2 standard, which represents realistic ESD transients encounter by electronic systems in field.

The TransZorb diode (1N6037) is studied for its clamping characteristics with standard test waveforms and ESD transient behavior. It has been observed that the device conforms to its breakdown voltage at steady state low frequency conditions as mentioned in the manufacturer’s data sheet. At frequencies greater than few MHz, attenuation provided by this device is more of filtering in nature, provided by capacitance of device than clamping by its breakdown.

Design transient protection circuit for very high-speed signal lines by taking into account of the capacitance and placement of ESD suppression devices with respect to the device to be protected.

6.0 References

1. “Human-Metal Electrostatic Discharge in IEC, ANSI and MIL Standards”, By Janusz Baran, Częstochowa University of Technology, Częstochowa, Poland, Jan Sroka, Warsaw University of Technology, IETiSIP, Warsaw, Poland. (www.interferencetechnology.com)
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