Abstract:

Today’s Printed Circuit Board (PCB) design challenges are not only confined to terrestrial PCB designs, but also extended to more prominent and critical Space-grade PCB. There are additional challenges due to Space environment and requirement of achieving high reliability PCBs beyond Class-3 with failure risk less than 0.001%.

This paper describes Space-grade PCB design issues, design flow, design guidelines and techniques. It also explains PCB design issues and critical tasks necessary for ensuring reliable Space qualified PCB.

1.0 Introduction

In recent time, because of advancement in chip-technology, PCB designs are undergoing revolutionary changes with respect to the size and weight while increasing the clock speeds on the board. With increasing use of high VLSI density devices like FPGA, ASIC etc., PCB design also becomes more and more dense, complex and challenging. These PCB design challenges include placement and routing of high pin count/fine-pitch components, handling of highly dense interconnections, blind/buried/microvias, electrical issues like Signal Integrity (SI), Power Integrity (PI), Electro Magnetic Compatibility (EMC) and thermal management.

Space-grade PCB encounters more or less same challenges as commercial-grade PCB designs, albeit with minor differences and additional challenges. The process of designing space qualified PCB is very critical and involves stringent design constraints. On the Earth, surrounding atmosphere protects the circuits from Space radiations that can cause a failure in the circuit. The well defined PCB guidelines and procedures have to be followed to meet the objective of a critical Space mission.

As the mainstream PCB design tools primarily focus on commercial-grade PCB designs, Space PCB specific tools are not available in the market. Hence, the PCB designer has to demonstrate through design practices and analysis that space borne PCBs will not encounter a failure.

The subsequent sections describe space-grade PCB issues and critical tasks, Electronics Computer Aided Design (ECAD) based PCB design flow, design techniques pertaining to component placement, routing, SI, PI, thermal management and EMC.

2.0 Space-grade PCB and its requirements

Terrestrial PCBs, for ground applications, are required to meet the intended functionality and performance where failure is tolerable since they are repairable, while in Space, failure is not an option. PCBs shall not only meet the intended functionality and continuous performance in harsh space environment but also ensure high reliability in high risk Space missions. Communication satellites, Remote sensing satellites, Navigational satellites and other planetary and earth observation space missions require highly reliable PCBs for their sophisticated instrumentations. Like commercial PCBs, space-grade PCBs are subject to thermal and mechanical stresses during their fabrication, soldering and assembly processes. In addition to these stresses, the Space-grade PCBs are subjected to shocks and stresses imposed during launch of space flights and required to perform intended function under Space radiation and vacuum conditions. The vacuum conditions make PCB heat dissipation difficult, if not managed properly, it may develop cracks in PTH and solder joint related problems.

On Earth, the circuits are protected by atmosphere from Space radiation containing high -charged particles. The charge particles deposited on spacecraft surface can penetrate in to the circuit board and may create Electro Static Discharge (ESD) threat. Hence, it is necessary to avoid objects that store and accumulate charge in the spacecraft. Isolated PCB copper and dielectrics like FR4, Kapton are excellent charge-storing materials, which should be avoided. Isolated copper, traces with greater than 0.3 cm$^2$ should be grounded and exposed dielectric PCB material shall be covered with solid copper connected to reference plane. Use of leaky conformal coating can provide automatic bleed path without affecting circuit operations. Moreover, depth-to-ground plane should be made as small as possible, less than 10 mils is preferred. Highly dense board are less susceptible to charged particles, so more care should be taken for low or moderate dense boards.
The most important factor for space hardware is the reliability. Since the electronics hardware is operational in space, it is not possible to repair these in case of failures, hence, it is necessary to attain nearly zero failure risk. Moreover, long life satellite missions require continuous performance of space electronics for several years without any technical glitch or downtime. And design of PCB can have direct impact on the reliability of Spacecraft. Any single failure in PCB can lead to the loss of a critical function of space mission. The high reliability requirements of Space PCB necessitate:

- Stringent PCB design guidelines
- Robust PCB design flow and techniques
- Use of Space grade components and suitable de-rating of stress levels of components
- Providing redundant circuits or circuit paths

### 3.0 Design Guidelines for Space PCBs

The well defined PCB design guidelines shall be rigorously followed for quality assurance in space projects and applications. The ISRO PCB guidelines address space-grade PCB requirements in terms of size, shape and tolerances of PCB material and copper patterns. At the same time, it also ensures sufficient margins for PCB fabrication, assembly and testing. The guidelines take care of PCB Design For Manufacturing (DFM), Design For Assembly (DFA) and Design For Testing (DFT) along with quality and reliability of space missions.

Following are main points of Space-grade PCB design guidelines that are more stringent and quiet different than traditional PCB guideline.

- Current carrying capacity of track shall be de-rated by 66% for onboard PCB. For commercial ground PCB, it is de-rated by about 25%. Track width is decided on basis of temperature rise due to current flowing through the track. In the space environment, the convection based heat transfer is absent due to vacuum, and hence, heat can be transferred only by means of conduction and radiation. Hence, the current carrying capacity of the conductor must be sufficiently derated.
- Wide conductors connecting to a pad area can act as solder thieves by drawing solder away from the pads and down to conductor. Further, if a conductor goes to a via, which is connected to an inner power-plane, the conductor may act as a heatsink and draw heat away from pad or component lead during soldering process resulting in a cold solder joint. Hence, conductor width of 1 mm, length of 1.5 mm and pad-to-track ratio 1.5:1 shall be used for such connections. Because of this reason, via-in-pad is not preferred for onboard PCBs.
- Minimum inter-card distance is required to be 3.5mm to meet vibration requirement
- Only through-hole and buried vias shall be used for flight model onboard PCB, blind vias are not permitted
- Only PTH is allowed; standoff, eyelets, rivets etc. are not allowed
- Only fixed value components are allowed. Trimpots, variable capacitors, variable inductors are not permitted in FM PCBs
- The build-up of PCB, which includes layer-stack, copper distribution and component placement, shall be symmetric to avoid warp and twist in the PCB
- Copper clad laminate construction shall be used. Laminate construction offers better peel strength than copper foil construction
- Solder mask is not preferred in onboard PCBs. Problem seen with solder mask include poor adhesion to tin-lead, poor outgassing performance, and high risk involved with selective stripping of tin-lead.
- All areas of conductive patterns and dielectric material shall have dimension of > 0.1mm, to prevent sliver and peelable.
- Conductors on external layers should be covered with conformal coating to avoid ESD threat and Paschen discharge that occurs during launch
- Critical nets should be routed on the same layer. If this is not possible, minimum vias shall be used along with second redundant track and via. This is necessary to prevent open circuit failure of a single interconnection.
- Screening tests for all the components is mandatory for onboard designs to remove non-conforming components, components with random defects or components likely to experience infant mortality. Radiation hardened active components and other space qualified discrete components may only be used for onboard designs.
4.0 PCB Design Flow for Space PCBs

The PCB design flow, shown in Figure 1, depicts design steps and methodology used to design space-grade PCBs.

As shown, initial electronic design concept is entered in an ECAD platform using Schematic Capture tool. A design can be entered either in flat or in hierarchical mode. In flat mode, every component and connection is added individually. In hierarchical design, sub circuit can be designed once and included in design as many times as we need. It allows number of engineers to work on the same design. It makes complex design in to manageable small blocks and reduces apparent complexity of design. The onboard schematic design conforms to the IEEE STD 315 for graphical symbols, IEEE STD 91 for logic symbols and IEEE STD 991 for logic circuit diagrams. The schematic diagram should be
logical, neat and clearly laid out from left-to-right as per signal flow and functionality of design. Engineering Rules Checks (ERC) such as gate overloading, mixed logic types, grounded source, shunted source, multiple sources, tri-state errors etc. should be carried out before generating the netlist for PCB. Pre-layout analysis typically includes creation of transmission line topology, as shown in figure 2, by adding sources, receivers, terminations and transmission lines. Experiments with different types of topologies like star, remote star, daisy etc can be carried out. These topologies can be simulated and most suitable topology can be assigned to critical high speed signals. It is also possible to extract transmission line topology from routed board for analysis. Pre-layout simulation helps to generate high speed design constraints such as signal delay, overshoot, undershoot, crosstalk level etc. for critical analysis.

![Figure 2: A typical transmission line topology](image)

PCB layout is a vital step which includes PCB material selection, pad stack and layer stack definition, component placement and trace routing. Padstack requires definition of pad size and shape for all electrical layers, solder mask and solder paste layers.

Layerstack design shall follow “homogeneous distribution” rule that applies to X, Y and Z axes for copper and dielectric material distribution. Heavy power and ground layers should be placed in symmetrical manner, close to centre of the laminate.

PCB material selection can have a major impact on performance of the RF/Analog and high speed digital circuits. RF/Analog circuits usually process precision low level signals, As a result, these circuits require much tighter control of parameter such as loss tangent, dielectric constant, dielectric thickness, trace width which affect signal quality. Usually the most suitable material for RF/analog design is PTFE that has lower loss tangent (0.0002- 0.002) – approximately 10 times lower than FR4.. Moreover, it has lower dielectric constant, half of FR4, so velocity of signal will be faster than FR4. Lower dielectric constant necessitates wide traces to get 50 or 75 ohm impedance value, resulting in lesser impact of skin-effect.

RF circuit designed in Agilent’s ADS can be imported in to PCB editor. Likewise, mechanical drawing and board dimension from MCAD package can be imported in to PCB editor. Library databases contain part details, PCB material properties, component IBIS and SPICE models, various PCB design technologies that define design rules, CAM detail, templates etc. To achieve flawless PCB design, the netlist comparison is carried out for Layout verses Schematic (LVS) in front end design and ECAD verses Electronics Computer Aided Manufacturing (ECAM) at back-end.

5.0 PCB Design and Associated Analysis Techniques

Design guidelines and standardf generally state minimum dimensions permitted. It is good practice to use minimum dimension only when necessary; otherwise optimal value higher than minimum value shall be used. For instance, it is necessary to use minimum track-to-track distance in high dense boards where there is no room, but in low or moderate dense board where there is enough room, fan out of track should be carried out for larger insulation distance between them.

Component Placement: Placement of component is the most important step of PCB design. It has got electrical, mechanical and thermal restrictions. A good component placement can reduce the overall length of connections, reduce the complexity of the routed connections, reduce number of vias, Improve reliability and manufacturability by providing balanced physical and thermal structure of the board. Component keep-in and keep-out areas shall be created with associated components that are either included or excluded from the area.. The component shall be placed in following order:
Component orientation has to be consistent. Wherever possible, all components should be placed either north/south or east/west position. In other words, the sides or longitudinal axes of components should be either parallel or perpendicular to one another. In rectangular or square board, component axes should be parallel to board edges. However, 45° orientation is possible. Pin-1 and polarity marking of components shall be aligned in increment mode from left-to-right and top-to-bottom. Accessibility clearance shall be kept for assembly, testing and rework. Enough spacing shall be kept around tall components, because they block vision in a conical area around them and may obstruct placement-head of ACM. Likewise enough spacing shall be kept around hot components and test points. Heat sensitive components shall not be placed near hot components. Decoupling capacitors must be placed within effective distance from active device. Paralleling capacitors is a common technique for lowering overall Equivalent Series Resistance (ESR) and Equivalent Series Inductance (ESL) of decoupling capacitor.

**PCB Trace Routing:** Grid setting is an important and foremost step for trace routing. Since all ECAD based routers are grid based, it is essential to set grid correctly for efficient and effective use of package. The routing grid should be multiple of system grid, component placement and via grid should be multiple of routing grid. 100 mil grid shall be set for placement of DIPs and through-hole components, 25mil or 50 mil shall be set for SMD components.

Woven PCB substrate is made of glass-fibers and epoxy resin, and glass-fibers have higher dielectric constant than the epoxy resin. And if a track lies predominately in a glass-rich area its impedance will be lower than the calculated value and if it lies over an epoxy-rich area its impedance will be higher than calculated value. This effect can create SI related problem, which can be mitigated by routing track at 45 degree to average out the effects of weave, as shown in below figure 3A.
Lengthening shall be used for critical nets to match exact lengths of traces and resolve signal skews and delay problems, figure 3B shows accordion kind of track lengthening with guarding on both the side.

Smoothing and Mitring of all routed tracks is necessary. Smoothing allows us to reduce number of vias, segments and also places the tracks more evenly. Mitring introduces 45 degree segment on orthogonal corners of tracks.

Ground Shielding should be used for critical sensitive nets that need to be protected from interference from other signals as shown in figure 3A and 3B.

Differential pair routing: High speed designs often have connections that must be coupled tightly and routed close together to maintain impedance. Differential pair routing shall be used for such kind of nets. Rule W < D <3W, 2D < H , where W= track width, D= spacing between two nets and H= height of dielectric, shall be followed.

Escape routing: Routing from high I/O area to low I/O area shall be used for fine pitch components and high I/O BGAs.

**PCB Analysis:** This involves SI, PI, EMI and thermal analysis of complete routed design. These analyses ensure electrical and thermal performance of board for intended function. To have better of PCB at high frequency, use of reference power plane is mandatory. Power planes reduce impedance which results in reduction in undesirable inductive noise like ground bounce. They add distributive capacitance, and act as decoupling capacitor at high frequency. Apart from reducing loop area of signal path which decreases EMI radiation, they also act as shield against external noise sources. It is important basic layout technique not to have any holes, slots or any kind of perforation in the ground plane, as it creates discontinuity in trace impedance and also inhibits RF return current.

**Signal Integrity:** As the frequency of operation increases, the wavelength of the highest harmonics of signal approaches the PCB conductor’s physical size and conductor starts acting as a transmission line and cause problems of signal reflection, ringing, and crosstalk.

Ringing and reflection occur due to mismatch or discontinuity in impedance and can be minimized by keeping trace width constant, using proper line termination and using continuous reference plane, that is, without perforation.

For minimizing intra-layer crosstalk, keep wide spacing between traces and decrease degree of parallelism among them. For inter-layer crosstalk, use orthogonal routing with traces running on one layer running in X-direction and traces running on another layer running in Y-direction and isolate layers by ground or power plane.

**Power Integrity:** In high speed circuits, voltage fluctuations affect timing budget in IC and may cause failure. Power distribution network of PCB must provide constant voltage on the IC pads and also provide low impedance path for supply. The voltage must be stable from DC up to the frequency of interest. Decoupling capacitors maintain the voltage within certain tolerances at supply pin of IC despite its fluctuating current demand. The decoupling capacitors and their distance from their respective chips, and values of these capacitors have major impact on power distribution network. These impacts can be analyzed and simulated using PI tools.

Low ESL, multilayer ceramic caps with reverse aspect ratio – width is more than its length, and multiple decoupling capacitor of appropriate value are required to be used. When one capacitor’s frequency response is rolling off, another’s becoming significant, thereby maintaining a low impedance over required frequency range

Power and ground planes should be kept close to each other so that they can create distributed capacitance and can be used as embedded decoupling capacitor to help achieve a low impedance power bus at frequency beyond GHz

**EMI:** The main sources of EMI radiations in PCB are: the “loop area” defined by a signal trace and its return path and pair of plane that resemble dipole antenna. The following techniques may be used to minimize EMI.

- Minimization of loop area
- 20-H rule shall be followed wherein ground plane shall be extended beyond power plane by 20 times the distance between them.
- Providing isolation between critical components and tracks by guarding and shielding, reducing signal reflection and crosstalk on high speed signals, using proper termination and decaps, grounding isolated copper area, putting ground vias along critical track, using ground planes without slots, mitring all traces and removing Ts on traces
- Low speed signals such as Reset, Interrupt are more susceptible victims of EMI and need to be isolated from high speed signals and s connected through HF RC filter.
- Separating HF/RF section, HS digital section and LF analog section
- Routing critical circuits away from I/O circuits
• Forming a faraday cage around the critical conductive patterns using shielding enclosure and around components using guard ring. The cage is to be grounded to low impedance path.

**Thermal Management:** The primary objective of thermal management is to ensure that all components on the PCB are maintained within their allowable temperature limits. PCB is an essential element needed to dissipate the heat from the copper patterns and components and keep the board and its assembly cool.

PCB dielectric is a poor heat conductor. But copper is relatively good conductor of heat and can be used for heat sinking. On the other side, depending on the current passing through copper pattern, they can also become a heat generator. Therefore, proper trace width and thickness must be checked to ensure that the wattage being passed through conductor does not raise the temperature of trace above a safe value, which may increase the failure rate of a PCB. That’s why current passing through a copper trace is derated by 66% for onboard PCB.

Heat onboard is generated by high pin count ICs, power transistors, transformers and other components that draw large amount of current. For space-grade PCB, component that has to dissipate more than 1 watt power or leading to temperature rise of more than 10°C shall include heatsink or thermal conductive material. Otherwise, components heat may make PCB hot and these may result in solder joint problems because of CTE(x,y) mismatch of PCB material and component or it may crack PTH due to mismatch in CTE(z).

Special metal-core plane shall be included to remove heat from PCB. Heat is transferred to metal core plane through thermal vias. These vias shall not be used for electrical connections.

**Criterion for RF PCB design:** The following PCB guidelines are to be followed in RF designs.

• Amplifier and filter inputs and outputs should be kept well separated and running in opposite direction maintaining their impedance
• Shield low level RF signals by pouring copper along its path
• Vias are to be avoided or minimized
• Orthogonal route is not allowed
• Use of minimum layers.
• Provide thermal relief pads to ensure reliable soldering
• Place ground vias on the both side of sensitive trace

**6.0 Conclusion**

Since failure is not an option in the Space grade PCBs and it has to endure hostile space environment, it is mandatory to design flawless PCB. Highly reliable PCB can be designed by following stringent space design guidelines, robust PCB design flow and effective design techniques. Design process shall accomplish electrical requirements, mechanical and thermal requirements of the circuits. Moreover, the design shall also take in to considerations DFM, DFA and DFT constraints of space-grade PCBs.

**References**

1. ISRO-PAX-301 PCB Design Guide line
2. IPC-2221A, IPC-2222 standards
3. High Speed PCB design Techniques by M V Shah and D. J. Bhatt

Mr. D. J. Bhatt has worked over 20 years in Space-grade PCB design and analysis at Space Applications Centre (ISRO). He is Engineer-in-charge of -ECAD department and focal person for onboard and ground based PCB designs of satellite payloads. His wide range of PCB design experience span over right from DC/Analog to high speed/RF PCB designs, and well versed in SI, thermal EMI/EMC, PI analyses techniques. He was responsible for establishing ECAD centre and has exposure to almost all PCB design software viz. Cadence, Zuken, Mentor Graphics etc.