IPC PCB Design Competition

GUIDELINES

Total Duration – 3 Weeks

#PCB Design

The PCB Design contest is planned to be conducted as multistage contest.

- **Semi Final Round** – at company premises (Apr – May)
- **India Region Final Round** – August 3, 2023, @ Hotel JW Marriot
- **Global Championship** – IPC HQ, Date-TBD

General Information

Design Contest will be held at Institution, Regional & National Level in stages with progressive increase in design intensity.

1. Design is executed offline, at participants' facilities
2. Contestants are given 3 weeks timeline to complete the design & submit the deliverables
3. EDA tools: Cadence Orcad/Allegro, Mentor Pads/Expedition, Altium, Zuken Cadstar.
4. IPC inputs are supplied Schematic in Orcad format, netlist and BOM.
5. The scope of design is from netlist import – Layout Design including library creation , output generation.
6. Executed Layout is a non- functional representative of design with state of the art parameters.
7. The contest will recognize the best designers from the region.Winner & Runner of the contest will be eligible to participate for second level evaluation.
8. The contestants will be judged on the following criteria :
    a. CAD tool expertise
    b. Perception of design technology and application will be bench marked against IPC 2221,2222,7351B,6012.
    c. Thoughtfulness to consequences of design constraints on down-stream yield in Fabrication, Assembly and Test
    d. Design Constraints with respect to interfaces
    e. DFx principles (DFM, DFA, DFR, and Design For Cost)
    f. Reliability Aspects
    g. Outputs compatible to IPC Connected Factory Exchange Program.

Design Instruction

1. Design is IPC Class-2 (Dedicated Service Electronic Products)
2. Library footprint shall be created using IPC 7351B standard - Level B (Moderate design complexity – Standard)
3. Assembly on both sides, design envelop restrictions need to be considered
4. Data Sheet shall be referred for the layout guidelines.
5. Grid placement & routing will be given weightage
6. Mechanical drawing will be provided in pdf format
7. EMI/EMC considerations, meeting crosstalk, signal integrity requirement are important constraints
8. No pin swapping allowed
9. All DRCs with respect to components, shapes, traces, area rules should be cleared and validated
10. Vias to be tented
11. Board is Rohs compliant
12. Standard Fabrication notes need to be added in the given template
13. IPC 2581 format is preferred, in addition to RS274X Gerber Data.

----------Thank You ----------